REMARKS

Summary of the Office Action

Claims 1-4, 15-18, and 29-32 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Seltzer et al. U.S. Patent No. 4,833,651 ("Seltzer") in view of Williams et al. U.S. Patent No. 5,084,841 ("Williams").

Claim 5 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Seltzer in view of Williams and further in view of M. M. Mano, Computer System Architecture, Prentice-Hall, Inc., pp. 97-98, 1976 ("Mano").

Claims 6-14 and 33-35 were objected to as being dependent upon a rejected based claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 19-28 were allowed.

Summary of Applicants' Response

Applicants note with appreciation the indication of allowable subject matter in claims 6-14 and 33-35. Applicants hereby expressly reserve the right to these claims in independent form, to the extent applicants have not already done so, if the base claims are ultimately not allowed.

Applicants respectfully traverse the rejections under 35 U.S.C. § 103(a).

Reply to Rejections Under 35 U.S.C. § 103(a)

Applicants respectfully submit that the combination of Seltzer and Williams fails to render obvious the claimed invention.

"A claimed invention is unpatentable if the differences between it and the prior art 'are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art.'" 35 U.S.C. § 103(a); *Graham v. John Deere Co.*, 383 U.S. 1, 14 (1965). Measuring a claimed invention against the standard established by section 103 requires the oft-difficult but critical step of casting the mind back to the time of the invention, to consider the thinking of one skilled in the art, guided only by the prior art references and the then-accepted wisdom in the field. *W.L. Gore & Assoc., Inc. v. Garlock, Inc.* 721 F.2d 1540, 1553.

The Examiner has suggested that the combination of the elements in Seltzer and Williams renders the claimed invention obvious. Applicants respectfully disagree and submit that there is no suggestion in the art that the references should be combined to provide a "first-in/first-out memory circuit" (claim 1) having a "shift register circuitry shifting in write data words in synchronism with the write clock signal" (claim 1) implemented in a "programmable logic device" (specification, p. 3, lines 6-7). Both Seltzer and Williams are directed at RAM-based FIFO memories that have dedicated RAM devices with FIFO characteristics. In contrast, the present invention is directed to a FIFO memory implementation in a programmable logic device "PLD" using 5 simple circuit components (FIG. 1), including shift register circuitry 60 shown in FIGs. 1 and 5.

Further, even if the references could be combined, they would still be confined to a FIFO memory implementation

using a dedicated RAM device. They would neither teach nor suggest the claimed elements of a "shift register circuitry shifting in write data words in synchronism with the write clock signal" (claim 1).

Seltzer discloses a "No-Fall-Through, First-In-First-Out memory which includes a dual port random access memory having a storage section comprising a plurality of locations for storing data words" (Seltzer, col. 2, lines 60-63). The No-Fall-Through, First-In-First-Out memory "comprises a 64-word by 8-bit dual-port random access memory (RAM)" (Seltzer, col. 4, lines 59-60). The RAM includes both a "write port 30 which receives data words from an external source via inputs D and writes them into the RAM's storage section in response to a write clock input signal" (Seltzer, col. 4, lines 62-65) and a "read port 22 which reads data words from the RAM's storage section, in the same sequence as previously written, in response to a read clock input signal RC" (Seltzer, col. 4, line 66 to col. 5, line 1).

In addition, the RAM shown in Seltzer FIG. 1 includes two status inputs, "a write pointer value indicative of "the number of data words which have been written" (Seltzer, Abstract) and "a read pointer value indicative of the number of data words which have been read" (Seltzer, Abstract). The RAM also includes a control input ("WPE" shown in Seltzer FIG. 1) to control its internal operations. The control input is generated by control logic 24 (Seltzer, FIG. 1) in response to "the difference between the write pointer value and the read pointer value" (Seltzer, col. 5, lines 14-15) computed by

comparator 18 (Seltzer, FIG. 1) that "includes a subtractor section and a decoder section" (Seltzer, col. 5, lines 10-11).

Seltzer does not describe, teach, or suggest that its No-Fall-Through, First-In-First-Out memory can be implemented with a "shift register circuitry shifting in write data words in synchronism with the write clock signal" (instant application, claim 1). Nowhere in Seltzer is described such a shift register circuitry, nor is suggested that dedicated dual-port 64x8 RAM 12 (Seltzer, FIG. 1) can be implemented with a shift register circuitry (shift register 60, shown in FIG. 1 of the instant application) "designed to store and output eight-bit data words" (specification, p. 17, lines 26-27) with "eight subcircuits 62" (specification, p. 17, line 28, and FIGs. 1 and 5). Shift register 60 includes "FIFO WRITE DATA" input 16 (instant application, FIG. 1), "FIFO READ OUTPUT" 70 (instant application, FIG. 1), write clock input 70 (instant application, FIG. 1), and control input 50 (instant application, FIG. 1), wherein "master or slave latches of subcircuits 62 ... are ... selected in response to the selection control signals currently being output (via leads 50) by Gray code subtractor 40" (specification, p. 18, lines 3-6).

Furthermore, Seltzer does not describe, teach, or suggest implementing dedicated dual-port 64x8 RAM 12 (Seltzer, FIG. 1) without write pointer 16 (Seltzer, FIG. 1) and without read pointer 16 (Seltzer, FIG. 1). The shift register circuitry of the present invention (shift register 60, shown in FIG. 1 of the instant application) only requires a single control input, namely control input 50 (instant application, FIG. 1), in addition to the write output, read input, and write

clock input signals used for its FIFO operation. There is also no suggestion or motivation in Seltzer that the FIFO memory control should be implemented with the simple design of the present invention using Gray code counters (counters 20 and 30 shown in FIG. 1 of the instant application) and a shift register circuitry (shift register 40 shown in FIG. 1 of the instant application) that "is effectively a subtractor operating on Gray code or Gray-code inputs" (specification, p. 13, lines 31-32).

In fact, Seltzer teaches away from such implementation by pointing out that a shift register implementation of a FIFO memory "is limited by the fact that it is a 'fall-through' device" (Seltzer, col. 1, lines 53-54) since "[a] substantial period of time is required to cycle a data word through the register from its first input block to the output block. That is, a number of cycle times equal to the depth of the register are required to allow a data word to 'fall through'" (Seltzer, col. 1, lines 54-58).

Seltzer specifically teaches away from such register-based FIFO implementation by using a dedicated dual-port 64x8 RAM 12 (Seltzer, FIG. 1) "wherein data being written into the device propagates to the device outputs before the conclusion of the write cycle" (Seltzer, col. 2, lines 23-25). Seltzer also teaches away from a simple PLD implementation of a FIFO memory using Gray code counters and a shift register subtractor circuitry by implementing its FIFO memory with a dedicated RAM having a write pointer, a read pointer, and a control input in addition to the write output, read input and clock signals. The write pointer and read pointer shown in Seltzer FIG. 1 "are

synchronous binary incrementing counters" (Seltzer, col. 6, lines 6-7) that are used as inputs to the RAM itself. The Gray code counters of the present invention are only used as inputs to the shift register subtractor circuit (circuit 40 shown in FIG. 1 of the instant application) and not as inputs to the shift register circuitry used for storing data words (circuit 60 shown in FIG. 1 of the instant application).

The Examiner has suggested that replacing the binary counters of Seltzer with the Gray code counters in Williams would render obvious the present invention. Applicants respectfully disagree. Williams discloses a FIFO memory "with high speed status flag generating circuitry that is programmable and immune to operating conditions and process variations ... by providing gray code counters and storage registers to monitor the reading and writing operations" (Williams, col. 2, lines 30-36). Like in Seltzer, the FIFO memory in Williams is "RAM based" (Williams, col. 3, line 39). As shown in Williams FIG. 1A, "the FIFO 12 is situated between one system A, 11, which may be a high speed data processor that is in communication through FIFO 12 to another system B, such as a low speed cathode ray tube (CRT) terminal 15" (Williams, col. 3, lines 40-44). There is no suggestion in Williams that FIFO 12 (Williams, FIG. 1A) should be implemented in a PLD.

Furthermore, there is no suggestion in Williams that FIFO 12 should be implemented with "shift register circuitry shifting in write data words in synchronism with the write clock signal" (instant application, claim 1) based on a control input from a Gray code subtractor circuit (circuit 40, shown in FIG. 1 of the instant application). The Gray code counters

disclosed in Williams are part of "status generating circuit 14" (Williams, FIGs. 1A-B) and are used to "generate Full, Half-Full, Empty, Full - N, and Empty + N status flags" (Williams, col. 3, lines 10-11).

There is no suggestion or motivation in Williams to use Gray code counters 16 and 19 (Williams, FIG. 1B) and comparator and logic circuitry 28 (Williams, FIG. 1B) to generate a control signal like control signal 50 shown in FIG. 1 of the instant application. Control signal 50 is used in the instant application to select "master or slave latches" (specification, p. 18, lines 3-4) of a shift register circuitry (circuit 60, shown in FIG. 1 of the instant application) used to store data words in a FIFO configuration. In contrast, the Gray code counters and comparator circuit disclosed in Williams are used simply to generate status signals for the memory, and not for "selecting for output a first data signal in the shift register circuitry based on the second data signal" (instant application, claim 29).

Additionally, Williams teaches away from using a shift-register-based FIFO implementation in favor of a dedicated RAM because "shift registers that serially write digital words therein at a desired speed and read serially therefrom at a different speed ... are of limited storage and have unacceptable delay times" (Williams, col. 1, lines 45-49). The lack of means for providing a FIFO memory that is implemented with "shift register circuitry shifting in write data words in synchronism with the write clock signal" (instant application, claim 1) based on a control input from a Gray code subtractor circuit (circuit 40, shown in FIG. 1 of the instant

application) in any of the prior art references is a strong indication that those means were not obvious at the time the invention was made.

Therefore, because there is neither suggestion nor motivation to combine Seltzer and Williams and because the combination of Seltzer and Williams fails to disclose all the limitations of claims 1-35, applicants respectfully submit that claims 1-35 distinguish from, and are allowable over, the cited references.

Conclusion

Applicants respectfully submit that claims 1-35 are in condition for allowance, and respectfully request the same.

Respectfully submitted,

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